Monte Carlo and Thermal Noise Analysis of Ultra-High-Speed High Temperature Superconductor Digital Circuits

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Abstract- **We model the high temperature superconductor (HTS) rapid single flux quantum (RSFQ) toggle (T) flip-flop including process variations and thermal noise. A Monte Carlo method is used to calculate the theoretical yield of the circuit at speeds ranging from 1 – 83 GHz and for various process parameter spreads. Thermal noise is also included in the simulations and we calculate bit error rates at 1 – 150 GHz as a function of temperature. Our results demonstrate quantitatively the difference between HTS layouts with and without parasitic inductance. Furthermore, our simulations suggest that using the existing HTS process with a 250 μV I_cR_n product the T flip-flop operating temperature should be below 40 K in order to obtain bit error rates less than 10^{-6} at gigahertz speeds.**

I. INTRODUCTION

In the decade since the discovery of high temperature superconductors there have been rapid advances in superconducting digital electronics. Using low temperature superconductors (LTS) complex Rapid Single Flux Quantum (RSFQ) logic circuits, comprising thousands of Josephson junctions, have been demonstrated at speeds up to 11 GHz [1]. Thus far, however, only small RSFQ circuits composed of 10-20 Josephson junctions have been demonstrated using high temperature superconductor (HTS) materials [2]. The demonstration of complex HTS RSFQ circuits has been impeded by fabrication and design difficulties with the high temperature ceramic materials. Specifically, the process spreads of HTS Josephson junction critical currents tend to be large (standard deviation equal to 10% at best) [3], and RSFQ circuits are sensitive to inductance variations, which may also be functions of the HTS process. These process variations can significantly degrade circuit margins and prevent complex circuits from working correctly.

We are therefore using Monte Carlo simulations [4] to analyze RSFQ circuits consisting of 100 junctions or less that are candidates for implementation in HTS. In the present work we focus on the toggle, or "T", flip-flop circuit which has successfully been demonstrated at 65 K by A. Sun and co-workers using a multilayer HTS process [2]. Our Monte Carlo analysis takes into account the process variations of the Josephson junctions, inductors, and resistors. We have also incorporated thermal noise into our SPICE simulator, and we calculate bit error rates (BER) as a function of temperature. Note that leakage current effects are specifically neglected in all simulations.

Figure 1a is a schematic circuit diagram of the HTS T flip-flop circuit fabricated by TRW [2]. The circuit includes parasitic inductances on all Josephson junctions and ground contacts. Figure 1b is an ideal toggle flip-flop without parasitic inductances, which was optimized by S. Kaplunenko at Conductus [5]. Our Monte Carlo and BER simulations compare and contrast these two circuits in order to quantify the effect of parasitic components.

Figure 2 is a WRspice [6] simulation of the circuit in Fig. 1a with a 10 GHz input and 4.2 K thermal noise. The first trace is the voltage input at node (1) in Fig. 1a, and trace three and four are the frequency divided outputs at nodes (3) and (4). The last trace is the voltage output from the SFQ-dc converter. The simulation clearly shows the operation of the circuit as it "flips" between the two output states. The thermal noise in this simulation is discussed in detail in Sec. III.

In the following section we give the results of Monte Carlo simulations of the flip-flop circuits in Fig. 1 at frequencies of 1-83 GHz and with various process parameter spreads. Section III describes the thermal noise implemented in WRspice, and the tests we used to verify that the simulator was operating correctly. We use WRspice to calculate bit error rates due to thermal noise in Sec. IV. A brief summary and conclusion is given in the final section.
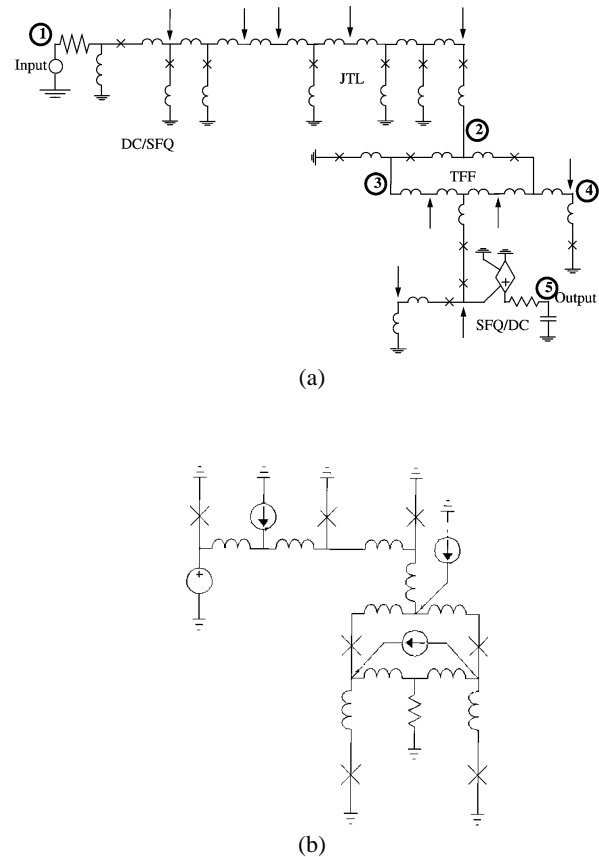

(a)

(b)

FIG. 1. (a) RSFQ T flip-flop circuit including parasitic inductance. (b) Ideal flip-flop with no parasitic inductance and no SFQ-dc converter at the output. The arrows denote dc bias currents.
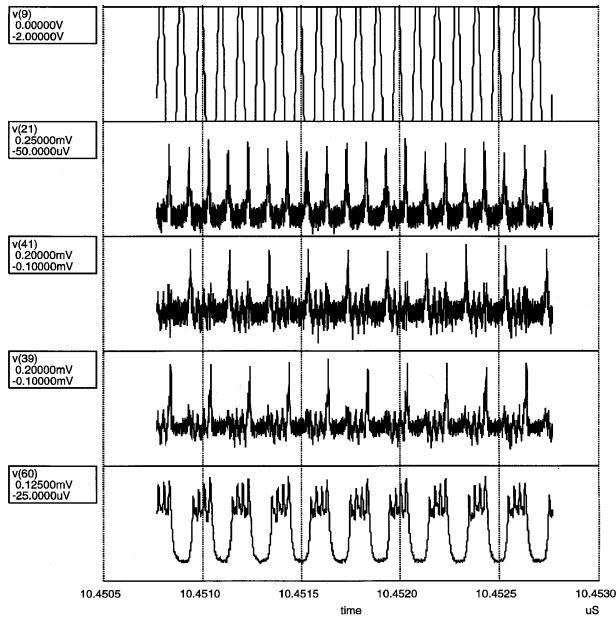
FIG. 2. 10 GHz simulation of the flip-flop circuit Fig. 1a with noise at 4.2 K.

II. MONTE CARLO SIMULATIONS

The theoretical yield for the circuits in Fig. 1 were calculated using a Monte Carlo simulation method [4] incorporated into WRspice [5]. The method includes both global (chip-to-chip) variations, and local (component-to-component) variations [4]. In the present work we focus on the process spreads given in Table I. These variations assume that the global spreads in critical current density J_c and normal resistance R_n are zero. This approximation is valid since in an HTS circuit experiment the temperature can be varied, so that global values of J_c and R_n are close to nominal. The inductance L will still have global variations resulting from variations of the HTS and insulator film thickness'.

Table I lists one standard deviation (1σ) variations defined for a generic process by TRW, Conductus, and Northrop Grumman HTS process experts. The first set of spreads are for an ideal process, similar to a present-day low temperature superconductor (LTS) process. The second set of spreads defines the present-day state-of-the-art HTS process. Finally, the "Medium" and "Large" spread parameters are of interest since they approximate the present-day average and worst case HTS process.

Figures 3a and 3b show Monte Carlo simulation results for the circuits in Fig. 1a and 1b respectively. For each case, theoretical yield was calculated for 100 Monte Carlo runs using the spreads given in Table I. With the ideal process, the

TABLE I
#### 1σ PROCESS SPREADS USED IN MONTE CARLO SIMULATIONS

Process Variations*	J_c	R_n	L
Ideal (~LTS)	5%	2.5%	5%
Present HTS state-of-the-art	10%	5%	15%
Medium spreads	15%	10%	10%
Large spreads	25%	15%	20%

*Local variations. Global variations are zero for J_c and R_n, 15% 1σ for L

probability of obtaining working circuits is high at 1 GHz, with 92% (+/- 4.8%) yield. However, this yield drops to 42% (+/- 9%) at 10 GHz. The circuit in Fig. 1a was optimized, including the parasitic inductors, for speeds less than 1 GHz. Optimization at higher speeds may improve the theoretical yields at 5 and 10 GHz.

The circuit yield in Fig. 3a is acceptable for the state-of-the-art HTS process; at 1 GHz the yield is 70% (+/- 8.3%). The yields at higher speeds are somewhat marginal; the 5 GHz yield is 40% (+/- 8.9%) and the 10 GHz yield is 12% (+/-5.8%). For the larger spreads the yield drops significantly, i.e. with the Medium spreads given in Table I at 1 GHz the yield is 46% (+/- 9.1%). Note that the simulations do not take into account the fact that in the experiment one can adjust bias currents. However, we do assume that the J_c and R_n global variations can be trimmed to zero by varying the temperature.

Figure 3b shows the calculated theoretical yield for the ideal flip-flop circuit Fig. 1b, which does not include parasitic components. This yield is a significant improvement over the circuit Fig. 1a. As an example, for the state-of-the-art process the yield is 83.5% (+/- 6.8%) at 50 GHz, and does not degrade significantly up to speeds of 70 GHz. Even with large spreads, the circuit has a 44% (+/- 9%) yield at 30 GHz. These results show quantitatively that parasitic inductance
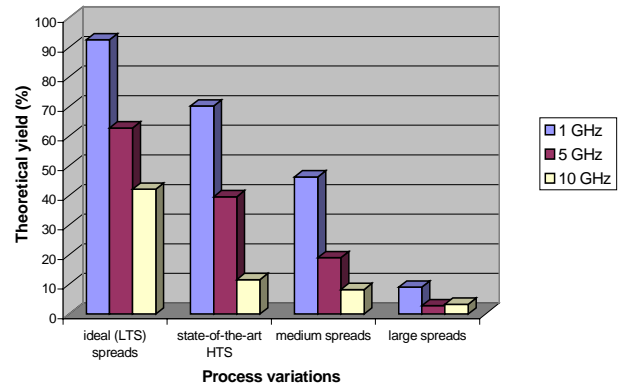
(a)
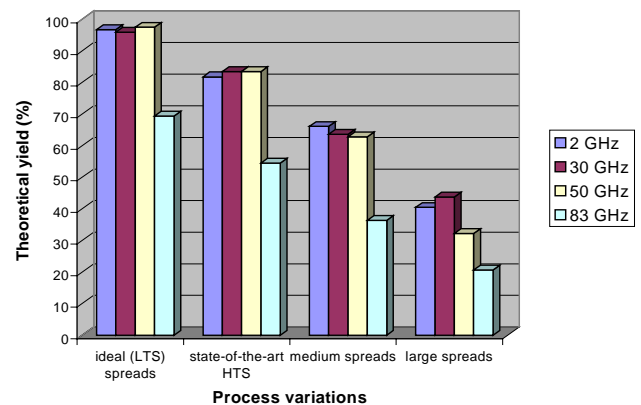
(b)

FIG. 3 (a) Monte Carlo yield results for the circuit Fig. 1a, with the parameter spreads listed in Table I. (b) Yield results for the ideal circuit Fig. 1b with no parasitic inductance. There is no noise in these simulations.

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can have a significant effect on the probability of obtaining working HTS RSFQ circuits at ultra-high speed.

III. WRSPICE SIMULATOR WITH THERMAL NOISE

We have incorporated thermal noise into the WRspice commercial Josephson SPICE simulator [6]. The noise is implemented at the source code level, and therefore the WRspice simulator should have a speed advantage over other methods that add noise from an external file [7].

Thermal noise, also known as Nyquist or Johnson noise, is modeled in a circuit by random current sources in parallel with each resistor in the circuit. The rms of these current fluctuations is given by the Nyquist formula [8]

$$i_{rms} = \sqrt{\frac{4k_B T f_c}{R}} \qquad (1)$$

where k_B is Boltzman's constant, T is temperature, R is the resistance, and the cutoff frequency $f_c = 1/2\Delta$ where Δ is the spacing between random numbers. If the noise is bandwidth limited, i.e. output from a filter, f_c in Eq. (1) becomes the bandwidth of the filter.

Noise is implemented in WRspice through the gauss function defined in the WRspice file by

```
*@ define noise(r,t,dt,n) gauss(sqrt(4*boltz*t/(r*2*dt)), 0, dt, n)
```

This noise function is then applied in parallel with each Josephson junction and resistor. A typical call to the noise function in parallel to a junction is:

```
b1 1 0 4 ybco area=0.0625
I10 1 0 noise($Rval, $Temp, $tmin, $whichn)
```

where ybco is a call to the Josephson junction model, Rval is the resistance of the junction, Temp is the temperature, tmin is the step size Δ, and whichn is an integer which defines the type of noise, either first-order interpolated or piece-wise-linear steps. The Josephson junction has an intrinsic WRspice model that includes capacitance R_n and I_c throught the area of the junction

The SPICE simulator must calculate circuit transients at time intervals less than Δ. To ensure algorithm stability, WRspice interpolates the random noise function between successive Δ-spaced time points. Two interpolation schemes are used. The first makes the noise constant during each Δ interval. The second noise function is a first-order linear interpolation between points.

This first noise function therefore consists of square "steps" with step width Δ. This square noise was used by Satchel [7], in part since it is easier to input from an external file into JSIM, and Tesche and Clarke [9]. However, Jeffery has previously used cubic spline interpolated noise with good results [10,11]. Our simulations show that as long as the Δ time scale spacing of the noise is small compared with the time constants in the circuit, the output of the simulation is independent of the exact form of the input noise function.

Verification that the noise is correctly implemented in the simulator is important if the results of the simulations are to be used by other laboratories. The WRspice simulator with thermal noise and Josephson junctions has been analyzed in detail. Specifically, we have calculated the rounding of I-V curves due to thermal noise first reported by Ambegaokar and Halperin (AH) in 1969 [12]. Comparison with the AH thermal noise rounding is a good test to verify Josephson junction simulators including thermal noise which has been used by Tesche and Clarke [9], and Satchel [7]. Both authors report simulations in good agreement with the AH result.

Our calculation of the thermal noise rounding of the IV curve were identical to those given by Tesche and Clarke [9], and are within a few percent of the original AH values. Higher accuracy can be obtained by increasing the length of the averaged data sets. Identical results were obtained using linear interpolated or piece-wise constant noise, and the simulations were found to be independent of the cutoff frequency.

We incorporated noise into the WRspice simulator in order to calculate bit error rates. At low temperatures this will require simulations for large numbers of cycles before thermal noise errors are detected. The stability of the WRspice integration algorithm is therefore essential for long simulation times.

Figure 2 shows a WRspice simulation of the circuit Fig. 1a at 10 GHz with 4.2 K thermal noise. The figure shows the last 20 cycles after the simulator has run for 104,525 cycles. This simulation took approximately 2.5 days of CPU time using a Sparc 20 workstation. Note that the circuit output is stable, and is similar to the simulator output without noise. No thermal noise errors were detected during the simulation. For all of the BER simulations described in the following section we first simulated at 4.2 K to test algorithm stability and confirm that there are no thermal noise errors. Simulations in excess of 300,000 cycles show no thermal noise errors at 4.2 K and no signs of round-off error.

IV. BIT ERROR RATE CALCULATIONS

We have calculated the bit error rates due to thermal noise for the circuits in Fig. 1 assuming nominal parameters. Following Satchel [7], the error rate is determined by simulating until the circuit makes an error. The simulation is then iterated, approximately 25 times, and the error rate is calculated by dividing the number of errors (iterations) by the total number of cycles simulated [7].

Typical simulations were for a noise spacing $\Delta = 0.25$ ps, so that $f_c = 2$ THz. Identical results were obtained for $\Delta = 0.1$ ps or a cutoff frequency of 5 THz. The simulations are computationally intensive, because circuits with bit error rates less than 10^{-6} require simulations for 10^6 or more clock cycles. For example, for noise defined on a time scale of 0.25 ps, a circuit with a 10 GHz clock simulated for 10^6 cycles requires integration of the circuit equations for 4×10^8 steps. This is more than 4×10^8 matrix multiplications internal to the SPICE simulator! In order to calculate bit error rates for such long simulation times we use several SUN Sparc 20 and ULTRA workstations, where each workstation calculates the BER of one circuit at a given temperature.

The results of the BER simulations with thermal noise are shown in in Fig. 4 and Fig. 5. The top two curves in Fig. 4 are for the circuit Fig. 1a simulated at 10 GHz and for two different values of $I_c R_n$ (160 μV and 230 μV). The $I_c R$ product was increased by fixing J_c at the nominal value and

increasing R_n. The net effect is to reduce the BER, as seen by the 230 µV I_cR_n curve with triangular markers. At 40 K the BER with the 160 µV I_cR_n was 1.1×10^{-3}, and for the 230 µV I_cR_n case it reduces to 6.1×10^{-4}. This reduction in BER is because the rms. amplitude of the noise, given by Eq. (1), varies inversely with the square-root of the resistance.

The bottom curve (circular markers) in the plot is the BER for the circuit Fig. 1b simulated at 10 GHz with no parasitic components. This circuit had a BER of 1.6×10^{-4} at 40 K. The error rates for the simplified circuit without parasitic components are therefore reduced significantly compared to those for the circuit with parasitics, the top curves in Fig. 4.
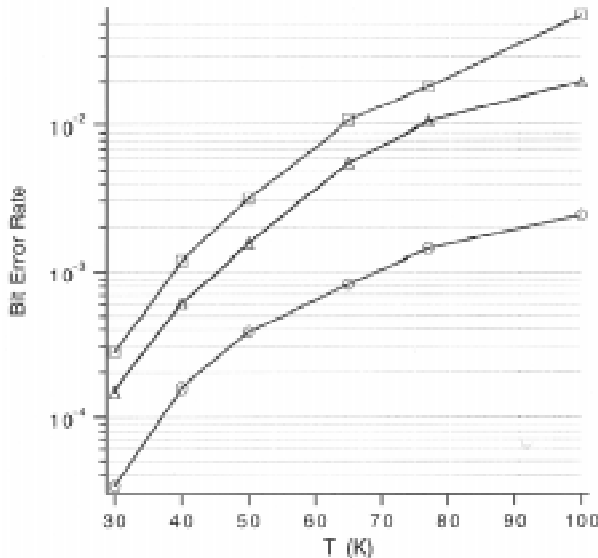

FIG. 4. BER as a function of temperature for the T flip-flop at 10 GHz. The two curves at the top are for the circuit Fig. 1a with an I_cR_n of 160 µV (square markers) and 230 µV (triangular markers). The bottom curve (circular markers) is the flip-flop Fig. 1b with no parasitic inductance.
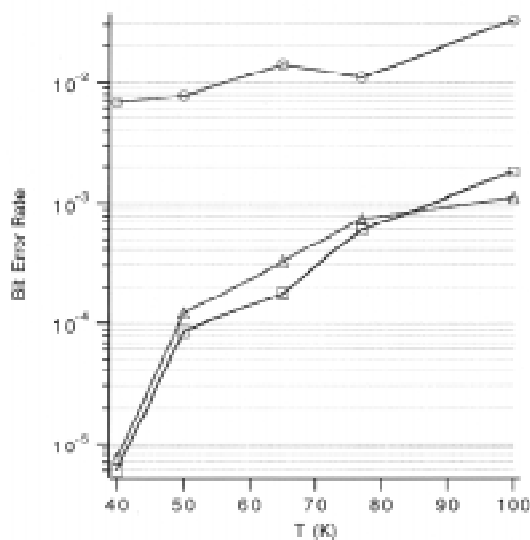

FIG. 5. BER calculated at ultra-high-speed for the T flip-flop Fig. 1b. The Top curve is 150 GHz, 500 µV I_cR_n. The bottom curves are 100 GHz (square markers) and 50 GHz (triangular markers), both for 250 µV I_cR_n product.

These results show that parasitic components can have a significant effect on the BER of HTS RSFQ circuits. Furthermore, to obtain BER less than 10^{-6} with the above circuit parameters and I_cR_n products, one must operate the circuits at less than 30 K.

We simulated the ideal circuit Fig. 1b at 50, 100, and 150 GHz, and with an increased I_cR_n product. See Fig. 5. The result was an improved BER for the 50 and 100 GHz cases. At 40 K the BER was 3.6×10^{-5} and 6.0×10^{-6} for the 50 and 100 GHz simulations respectively. The 150 GHz simulation was beyond the optimized range for circuit and the error rate was rather poor. With a 250 µV I_cR_n the ideal circuit performed well at 100 GHz and our simulations show that a BER much less than 10^{-6} should be obtained for temperatures less than 40 K.

V. CONCLUSION

We have used Monte Carlo and thermal noise simulations to analyze HTS T flip-flop circuits with and without parasitic inductances, and for different values of I_cR_n. Our simulations show that parasitic inductance terms can have a significant effect on theoretical yield and BER. Furthermore, increasing I_cR_n can also significantly improve BER providing the circuit is optimized accordingly.

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